ABSTRACT

A precision, low jitter oscillator circuit is provided that is particularly well-suited for generating a clock signal in miniature digital systems, such as digital hearing aids. The oscillator includes a plurality of differential inverters configured in a feedback loop to generate an oscillating clock signal. The differential inverters include a capacitive trimming network for adjusting the frequency of the oscillating clock signal and employ resistive loads for minimizing jitter in the clock signal. The components of the oscillator are fabricated in a common silicon process to minimize the size of the oscillator.